Electronic Version
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Claims

[c1] A method of fabricating a semiconductor structure, comprising:
forming a gate at least partially overlapping at least one source/drain region; and
forming a first step of material adjacent a side edge of the gate and forming a second step of material raised above the first step and remote from the side edge of the gate in a single material formation process.

[c2] The method of claim 1, further comprising depositing sidewalls on the edge of the gate.

[c3] The method of claim 2, further comprising etching a lower portion of the sidewalls to form an undercut.

[c4] The method of claim 3, wherein the etching comprises an isotropic etching.

[c5] The method of claim 3, further comprising forming the first step at least partially in the undercut.

[c6] The method of claim 4, wherein forming the first step and the second step comprises growing the first step and the second step.

[c7] The method of claim 2, wherein the second step is formed proximate to the sidewalls and remote from the gate.

[c8] The method of claim 1, further comprising forming a silicide on the second step and the gate.

[c9] The method of claim 1, wherein the first step is electrically connected with a portion of a conductive region arranged underneath the gate.

[c10] The method of claim 1, wherein the first step is spaced away from the side edge by a spacer.

[c11] The method of claim 1, wherein the first step and the second step are doped to form a raised source/drain region.

[c12] A method of forming a source/drain for a semiconductor device, comprising:
forming a first conductive region adjacent a side of a gate; and
forming a second conductive region at a height above the first conductive region.

[c13] The method of claim 12, further comprising arranging the first and second conductive regions above a third conductive region disposed within a substrate.

[c14] The method of claim 12, wherein the first conductive region is at a height of approximately 10 nm and the second conductive region is at a height above approximately 30 nm.

[c15] The method of claim 12, further comprising forming a spacer between a sidewall of the gate and at least a portion of the first conductive region.

[c16] The method of claim 12, further comprising the steps of: forming at least one sidewall adjacent the gate; and etching the lower portion of the at least one sidewall to form an undercut, wherein the first conductive region is formed at least partially within the undercut.

[c17] The method of claim 12, wherein the first conductive region and the second conductive region are formed in a single growing step.

[c18] A semiconductor structure, comprising:
a gate arranged to at least partially overlap at least one source/drain region;
a first step raised above a lower surface of the gate; and
a second step raised above the first source/drain step.

[c19] The structure of claim 18, wherein the first step is approximately 10 nm high.

[c20] The structure of claim 18, wherein first step and the second step comprise a single grown material.

[c21] The structure of claim 18, wherein a transition between an edge of the second step and the first step is a shape comprising one of a curved portion, an angled portion, and a stepped feature.

[c22] The structure of claim 18, further comprising a conductive layer arranged on a surface of the second step.

[c23] The structure of claim 18, further comprising the first step being arranged at least partially under an undercut formed in the sidewalls adjacent the gate.